CWBG
南方半导体

V_{DS}	1200V
$I_{D\ @25°C}$	79 A
$R_{DS(on)}$	25mΩ

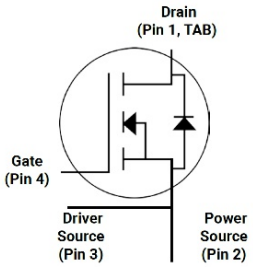
NF3M25120K

Silicin Carbide Power MOSFET
N-Channel Enhancement Mode

Features

- Benchmark gate threshold voltage
- High blocking voltage with low on-resistance
- High-speed switching with low capacitances
- Very low switching losses
- Halogen free, RoHS compliant

Package



Benefits

- Reduce switching losses and minimize gate ringing
- Higher system efficiency
- Reduce cooling requirements
- Increase power density
- Increase system switching frequency

Halogen-Free

RoHS

Applications

- Solar inverters
- EV motor drive
- High voltage DC/DC converters
- Switched mode power supplies

Part Number	Package	Marking
NF3M25120K	TO 247-4	NF3M25120K

Maximum Ratings (T_C=25ºC unless otherwise specified)

Symbol	Parameter	Value	Unit	Test Conditions	Note
V_{DSmax}	Drain-Source Voltage	1200	V	V_{GS} =0V, I_D=100μA	
V_{GSmax}	Gate-Source Voltage(dynamic)	-8/+19	V	Absolute maximum values	
V_{GSop}	Gate-Source Voltage(static)	-4/+15	V	Recommended operational values	
I_D	Continuous Drain Current	79	A	V_{GS}=15V, T_C=25 ºC	Fig.9
		66	A	V_{GS}=15V, T_C=100 ºC	
$I_{D(pulse)}$	Pulsed Drain Current	182	A	Pulse width t_p limites by T_{jmax}	Fig.22
P_D	Power Dissipation	250	W	T_C=25 ºC, T_J=175 ºC	Fig.20
T_J T_{stg}	Operating Junction and Storage Temperature	-55 to +175	ºC		
T_L	Solder Temperature	325	ºC		

Electrical Characteristics (T_C=25ºC unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	1200			V	V_{GS} = 0 V, I_D = 100 μA	
$V_{GS(th)}$	Gate Threshold Voltage	1.5	2.5	3.5	V	V_{DS} = V_{GS}, I_D = 10 mA	Fig.11
			1.8		V	V_{DS} = V_{GS}, I_D = 10 mA, T_J = 175ºC	
I_{DSS}	Zero Gate Voltage Drain Current			100	μA	V_{DS} = 1200 V, V_{GS} = 0 V	
I_{GSS}	Gate-Source Leakage Current			200	nA	V_{GS} = 18 V, V_{DS} = 0 V	
$R_{DS(on)}$	Drain-Source On-State Resistance		25		mΩ	V_{GS} = 15 V, I_D = 60 A	Fig.4,5,6
			30			V_{GS} = 15 V, I_D = 60 A, T_J = 175ºC	
g_{fs}	Transconductance		36		S	V_{DS}= 20 V, I_{DS}= 60 A	Fig.7
			38			V_{DS}= 20 V, I_{DS}= 60 A, T_J = 175ºC	
C_{iss}	Input Capacitance		4160		pF	V_{GS} = 0 V, V_{DS} = 1000 V f = 100kHz V_{AC} = 25 mV	Fig.17,18
C_{oss}	Output Capacitance		340				
C_{rss}	Reverse Transfer Capacitance		23				
E_{oss}	C_{oss} Stored Energy		292		μJ		Fig.16
E_{ON}	Turn-On Switching Energy (Body Diode FWD)				mJ	V_{DS} = 800 V, V_{GS} = -4 V/+15 V, I_D = 50 A,$R_{G(ext)}$ = 2.5Ω, L= 99 μH, T_j = 175ºC	Fig.25
E_{OFF}	Turn Off Switching Energy (Body Diode FWD)						
$t_{d(on)}$	Turn-On Delay Time				ns	V_{DD} = 800 V, V_{GS} = -4 V/15 V $R_{G(ext)}$ = 5 Ω, I_D = 60 A, L= 157 Inductive Load Timing relative to VDS Per IEC60747-8-4 pg 83	Fig.27
t_r	Rise Time						
$t_{d(off)}$	Turn-Off Delay Time						
t_f	Fall Time						
$R_{G(int)}$	Internal Gate Resistance		4.5		Ω	f = 100kHz, V_{AC} = 25 mV	
Q_{gs}	Gate to Source Charge		250		nC	V_{DS} = 800 V, V_{GS} = -4 V/15 V I_D = 60 A Per IEC60747-8-4 pg 21	Fig.12
Q_{gd}	Gate to Drain Charge		254				
Q_g	Total Gate Charge		423				

Reverse Diode Characteristics (T_C=25ºC unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions	Note
V_{SD}	Diode Forward Voltage		5.6		V	V_{GS} = -4 V, I_{SD} = 25 A, T_J = 25 °C	Fig.8,9, 10
			5.2		V	V_{GS} = -4 V, I_{SD} = 25 A, T_J = 175 °C	
I_S	Continuous Diode Forward Current		91		A	V_{GS} = - 4 V, T_C= 25 °C	
$I_{S,pulse}$	Diode pulse Current		182		A	V_{GS} = - 4 V, Pulse width t_P limited by T_{jmax}	
t_{rr}	Reverse Recover time		32.8		ns	V_{GS} = - 4 V, I_{SD} = 40 A,T_J = 25ºC, V_R = 800V	
Q_{rr}	Reverse Recovery Charge		122		nC	V_{GS} = - 4 V, I_{SD} = 40 A, T_J = 25ºC, V_R = 800V	
I_{rrm}	Peak Reverse Recovery Current		6.8		A	V_{GS} = - 4 V, I_{SD} = 40 A, T_J = 25ºC, V_R = 800V	

Thermal Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions	Note
$R_{\theta JC}$	Thermal Resistance from Junction to Case		0.6		°C/W		
$R_{\theta JA}$	Thermal Resistance From Junction to Ambient						

Typical Performance

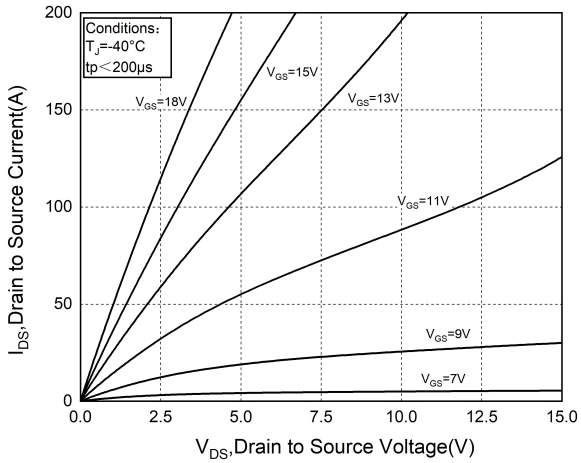


Figure 1. Output Characteristics TJ = -40 ºC

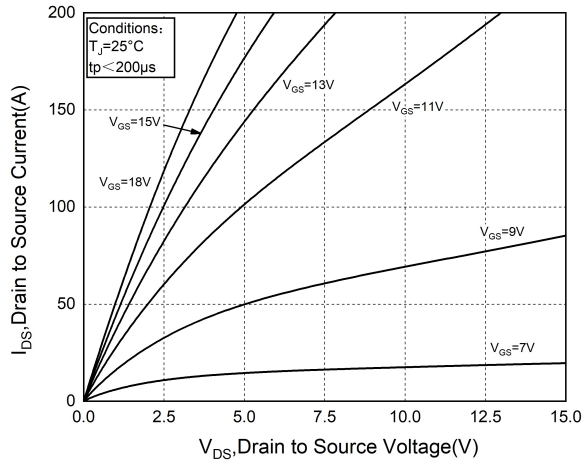


Figure 2. Output Characteristics TJ = 25 ºC

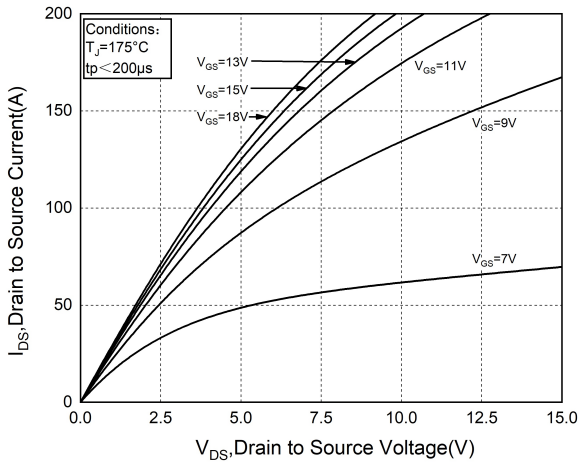


Figure 3. Output Characteristics TJ = 175 ºC

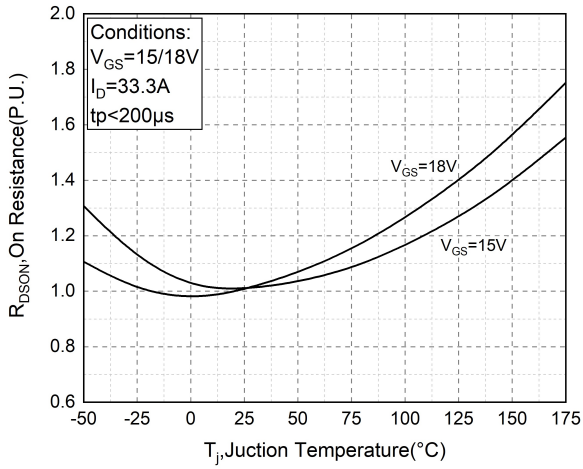


Figure 4. Normalized On-Resistance vs. Temperature

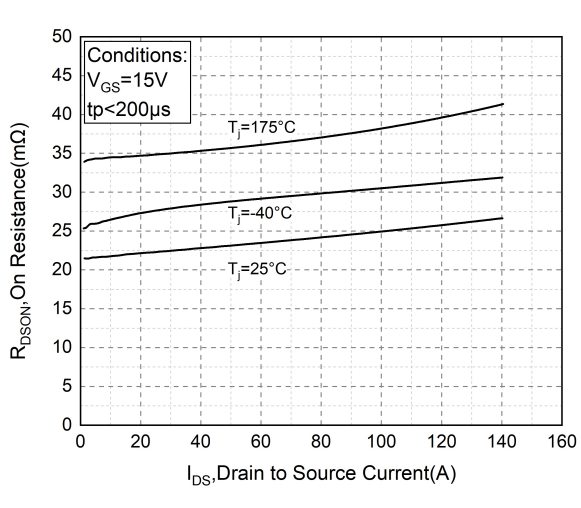


Figure 5. On-Resistance vs. Drain Current
For Various Temperatures

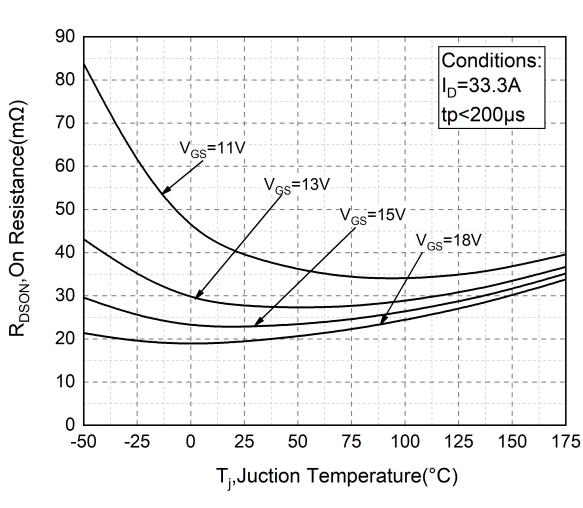


Figure 6. On-Resistance vs. Temperature
For Various Gate Voltage

Typical Performance

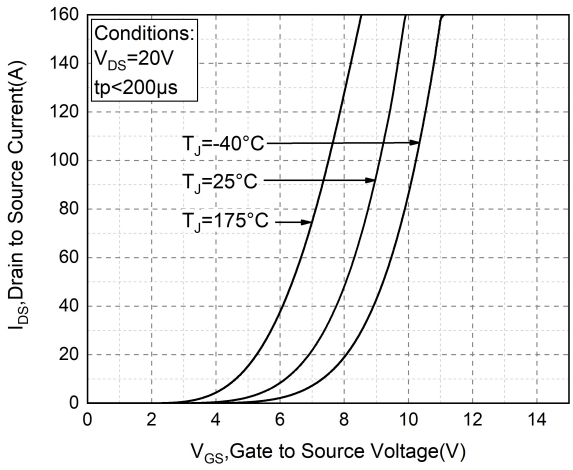


Figure 7. Transfer Characteristic for Various Junction Temperatures

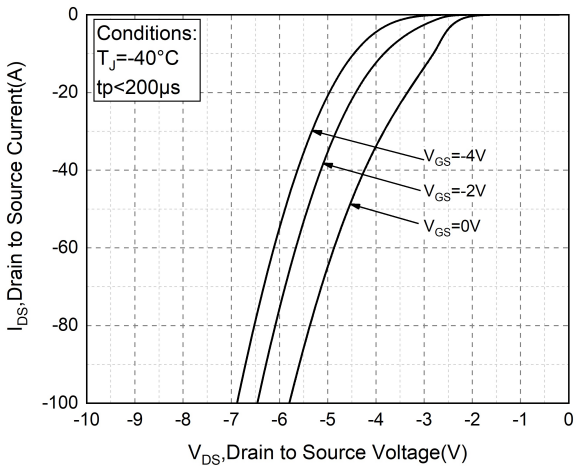


Figure 8. Body Diode Characteristic at -40 ºC

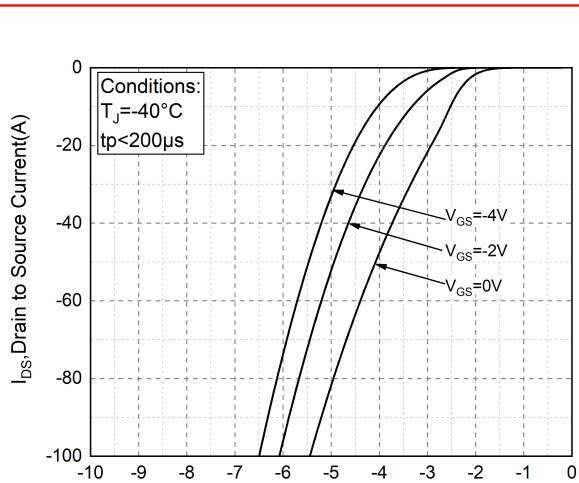


Figure 9. Body Diode Characteristic at 25 ºC

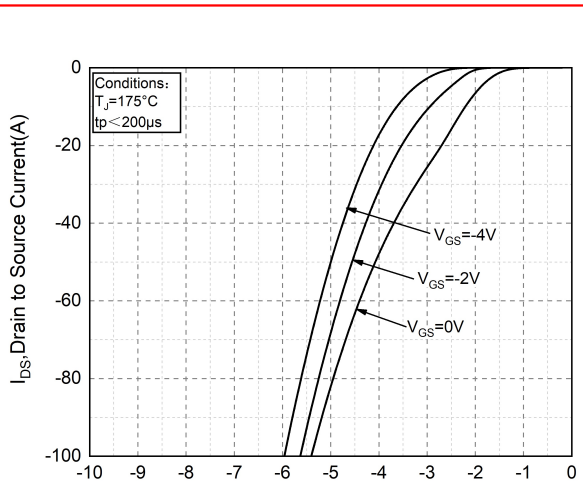


Figure 10. Body Diode Characteristic at 175 ºC

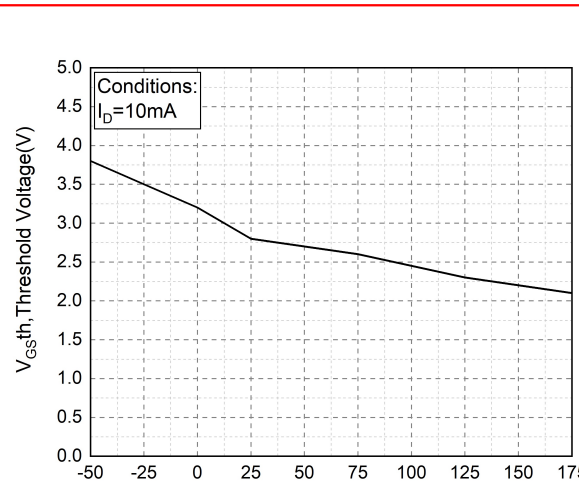


Figure 11. Threshold Voltage vs. Temperature

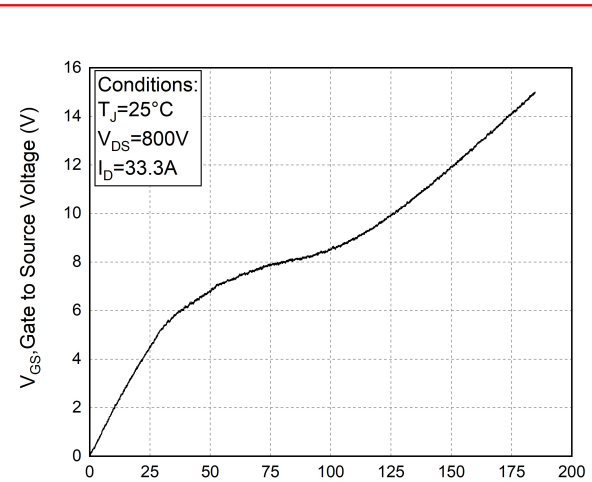


Figure 12. Gate Charge Characteristics

Typical Performance

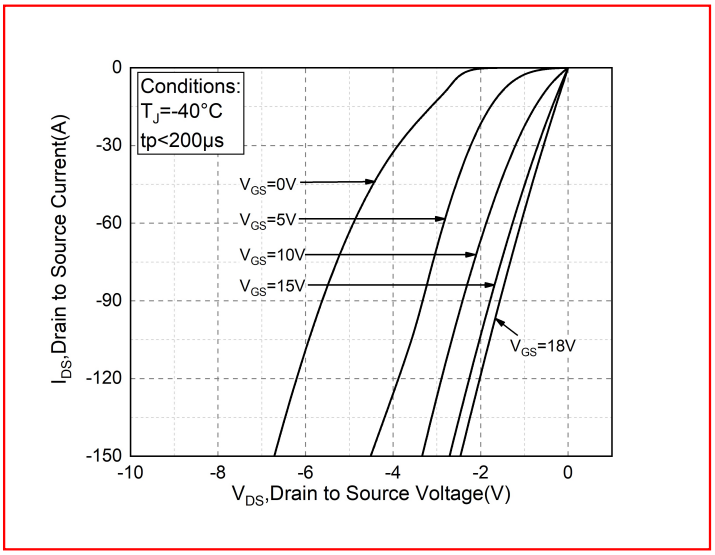


Figure 13. 3rd Quadrant Characteristic at -40 ºC

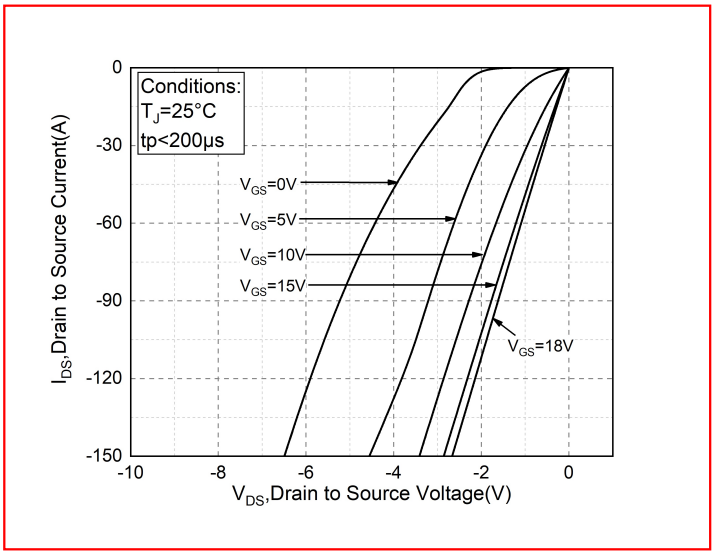


Figure 14. 3rd Quadrant Characteristic at 25 ºC

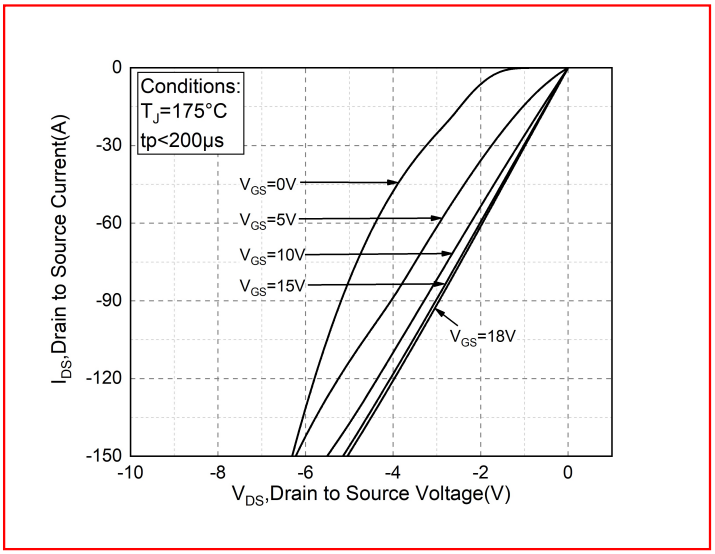


Figure 15. 3rd Quadrant Characteristic at 175 ºC

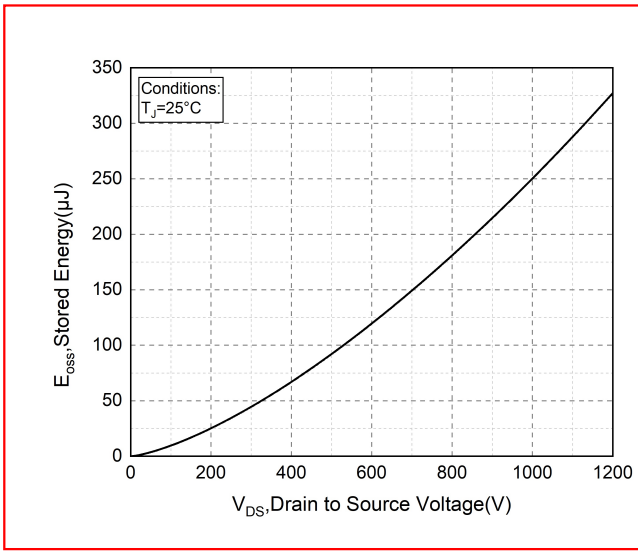


Figure 16. Output Capacitor Stored Energy

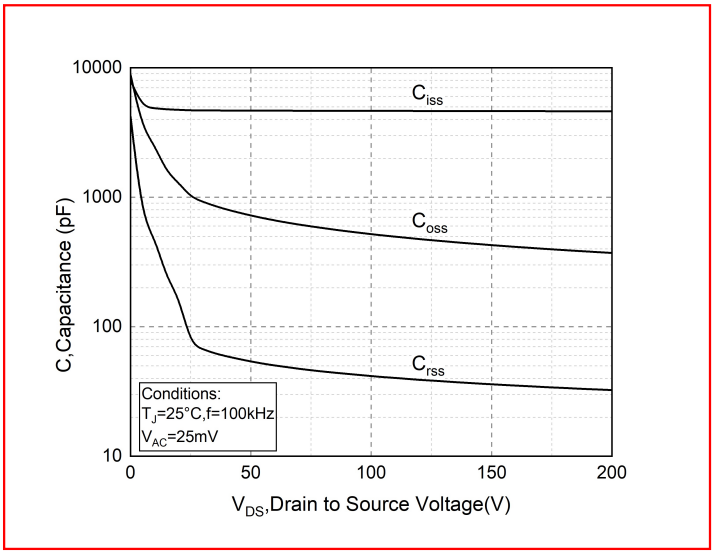


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200V)

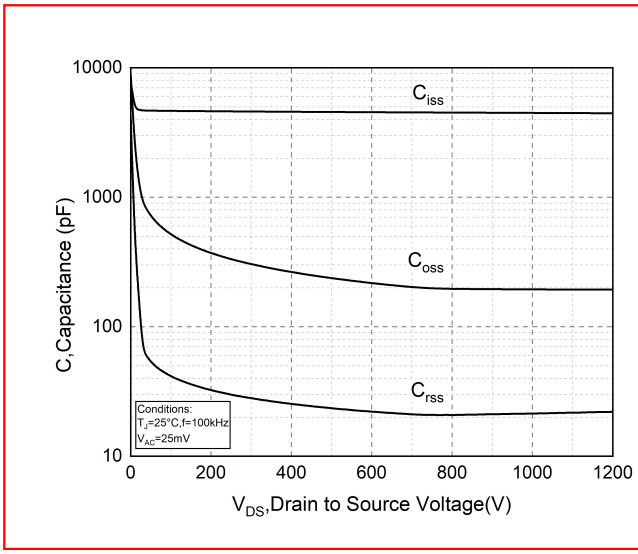


Figure 18. Capacitances vs. Drain-Source Voltage (0 - 1200V)

Typical Performance

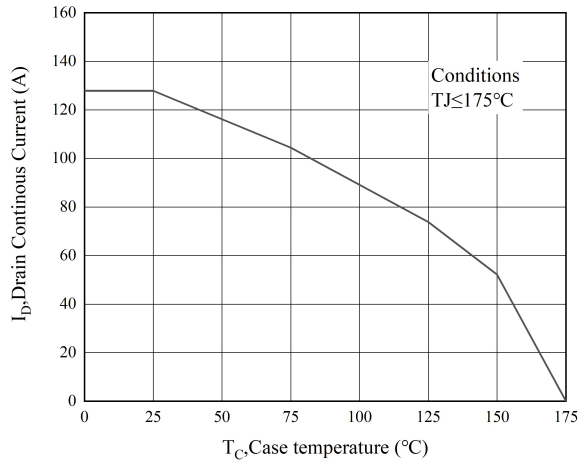


Figure 19. Continuous Drain Current Derating vs. Case Temperature

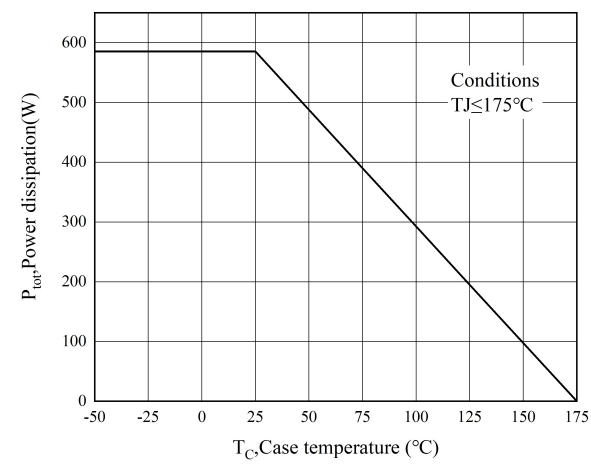


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

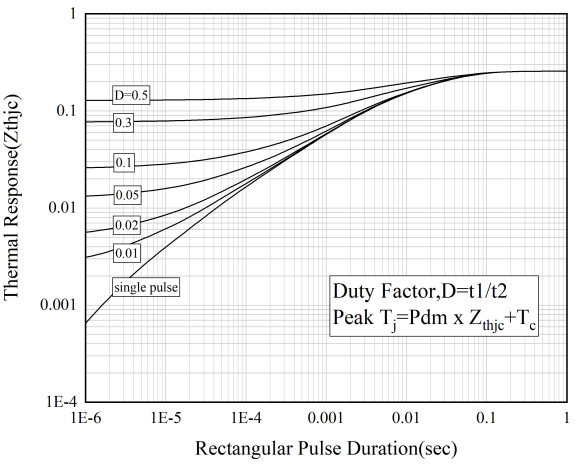


Figure 21. Transient Thermal Impedance (Junction - Case)

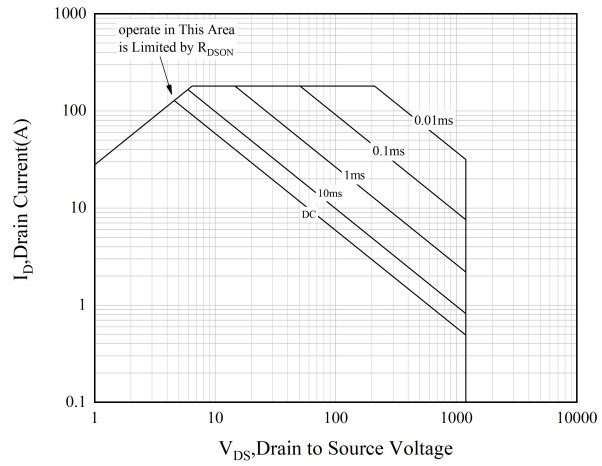


Figure 22. Safe Operating Area

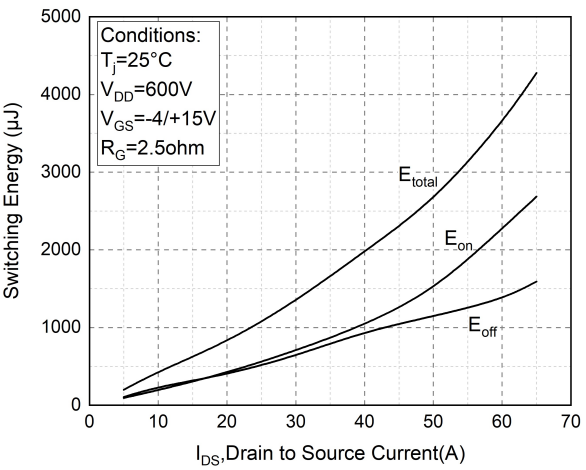


Figure 23. Clamped Inductive Switching Energy vs. Drain Current (VDD = 600V)

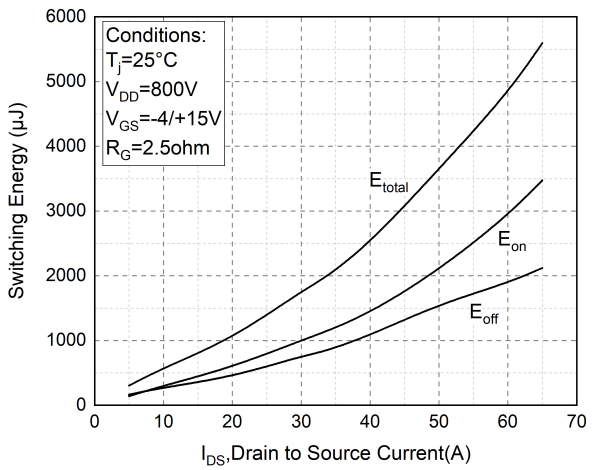


Figure 24. Clamped Inductive Switching Energy vs. Drain Current (VDD = 800V)

Typical Performance

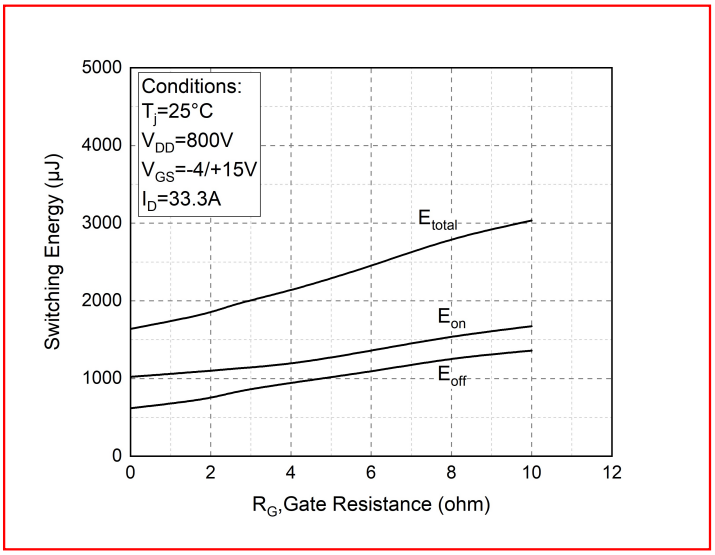


Figure 25. Clamped Inductive Switching Energy vs. $R_{G(ext)}$

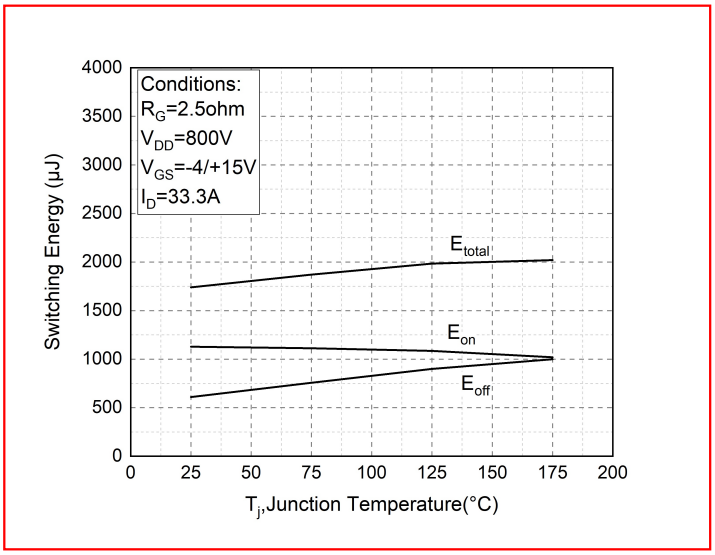


Figure 26. Clamped Inductive Switching Energy vs. Temperature

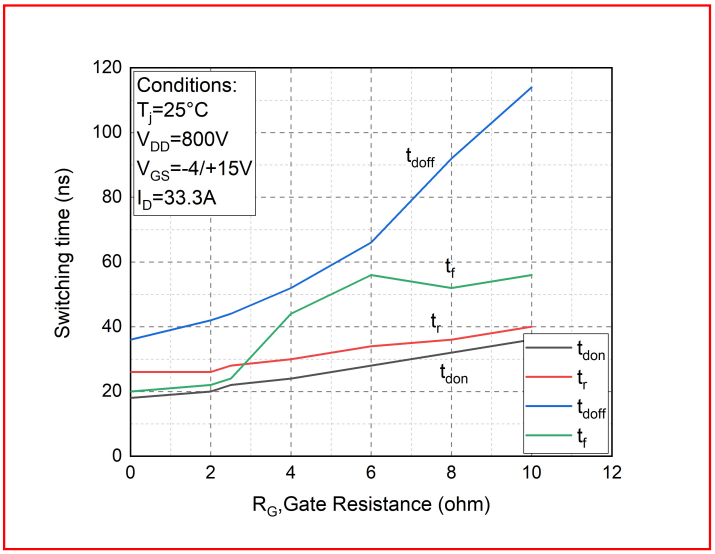


Figure 27. Switching Times vs. $R_{G(ext)}$

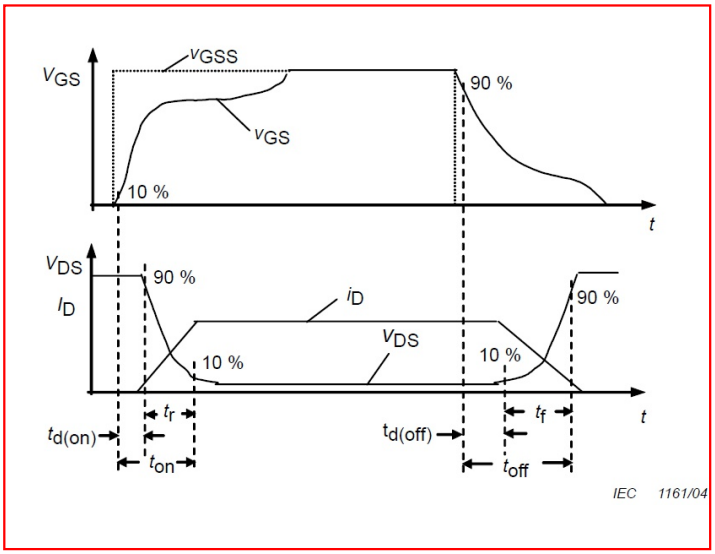
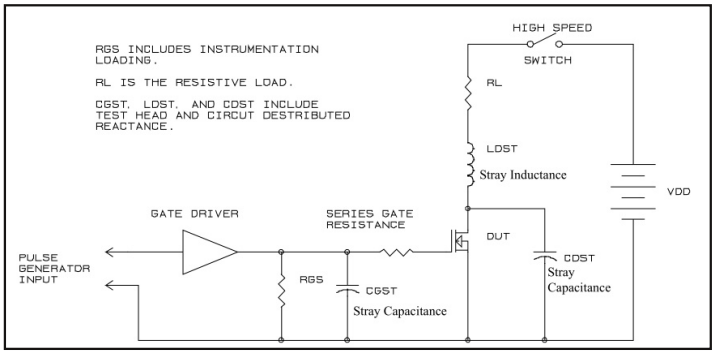


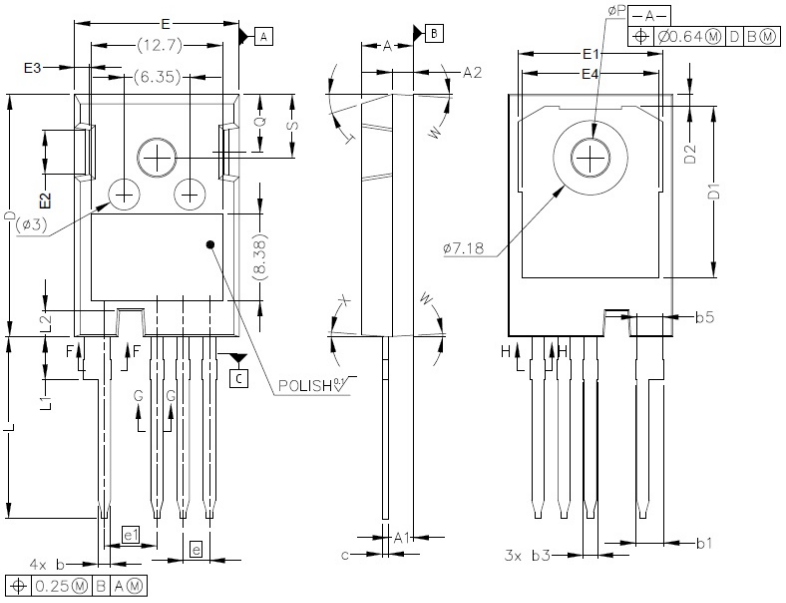
Figure 28. Switching Times Definition

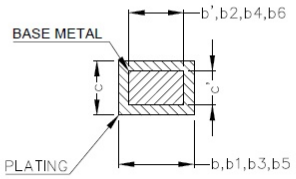
Test Circuit Schematic



Package Dimensions

Package TO-247-4





SECTION "F-F", "G-G" AND "H-H"
SCALE: NONE

SYMBOL	MILLIMETERS	
	MIN	MAX
A	4.83	5.21
A1	2.29	2.54
A2	1.91	2.16
b'	1.07	1.28
b	1.07	1.33
b1	2.39	2.94
b2	2.39	2.84
b3	1.07	1.60
b4	1.07	1.50
b5	2.39	2.69
b6	2.39	2.64
c'	0.55	0.65
c	0.55	0.68
D	23.30	23.60
D1	16.25	17.65
D2	0.95	1.25
E	15.75	16.13
E1	13.10	14.15
E2	3.68	5.10
E3	1.00	1.90
E4	12.38	13.43
e	2.54 BSC	
e1	5.08 BSC	
N	4	
L	17.31	17.82
L1	3.97	4.37
L2	2.35	2.65
øP	3.51	3.65
Q	5.49	6.00
S	6.04	6.30
T	17.5° REF.	
W	3.5 ° REF.	
X	4° REF.	

NOTE :
1. ALL METAL SURFACES: TIN PLATED,EXCEPT AREA OF CUT
2. DIMENSIONING & TOLERANCEING CONFIRM TO ASME Y14.5M-1994.
3. ALL DIMENSIONS ARE IN MILLIMETERS.
ANGLES ARE IN DEGREES.

Notes

Related Links